WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:

mounting a semiconductor chip, which has a main electrode and a subelectrode smaller in area than the main electrode on an upper surface thereof, on a die pad of an external lead frame through a first bonding material;

mounting an inner lead frame, in which a plurality of inner leads for connecting the main electrode and the subelectrode on the semiconductor chip to corresponding connecting pads of the external lead frame are joined together by a tie bar, on the semiconductor chip and the external lead frame through a second bonding material;

heating the first and the second bonding material simultaneously for electrically connecting and fixing the semiconductor chip to the die pad and the inner leads to the electrodes on the semiconductor chip and the connecting pads of the external lead frame; and

cutting the tie bar to separate the inner lead frame into the plurality of inner leads.

2. The method according to claim 1, further comprising the step of, subsequent to the step of mounting the inner lead frame, connecting a portion of the inner lead frame to another die pad of the external lead frame through a third bonding material.

3. The method according to claim 1, wherein the first bonding material includes one of soldering paste and conductive adhesive.

4. The method according to claim 1, wherein the second bonding material includes one of soldering paste and conductive adhesive.

5. The method according to claim 1, wherein the third bonding material includes one of soldering paste and conductive adhesive.

6. The method according to claim 1, wherein the first and the second bonding material include the same material.

7. The method according to claim 1, wherein the first and the third bonding material include the same material.

8. A semiconductor device comprising:

a plurality of external leads;

a die pad adjacent to the plurality of external leads;

a semiconductor chip mounted on the die pad and having a main electrode and a subelectrode smaller in area than the main electrode; and

two inner leads for connecting the main electrode and the subelectrode on the semiconductor chip to corresponding connecting pads of the plurality of external leads, the two inner leads having a tie bar cut.

9. The semiconductor device according to claim 8, wherein the tie bar is made smaller in thickness than other portions of the inner leads.

10. The semiconductor device according to claim 8, wherein the tie bar is provided midway on and between the external leads to which the two inner leads are connected.

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11. The semiconductor device according to claim 8, wherein the tie bar has a plurality of sub tie bars.

12. The semiconductor device according to claim 8, wherein the die pad has a notch in a portion that faces the tie bar.

13. The semiconductor device according to claim 8, wherein the two inner leads have tie bar portions thereof formed higher than a top of the semiconductor chip.

14. The semiconductor device according to claim 8, wherein the semiconductor chip includes a MOSFET.

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15. A semiconductor device comprising:

a plurality of external leads;

a first and a second die pad placed side by side adjacent to the plurality of external leads;

a first and a second semiconductor chip each having a main electrode and a subelectrode smaller in area than the main electrode;

two pairs of inner leads for connecting the main electrode and the subelectrode on each of the first

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and the second semiconductor chip to corresponding connecting pads of the plurality of external leads, each pair of the inner leads having a tie bar cut;

a protruding lead portion formed vertically on one side of the first die pad which faces the second die pad; and

a connecting lead portion formed integrally with one of the inner leads which is connected to the main electrode on the second semiconductor chip mounted on the second die pad and having a notch engaged with the protruding lead portion so that the connecting lead portion and the protruding lead portion are electrically joined together.

16. The semiconductor device according to claim 15, wherein the protruding lead portion has a flat portion in an upper portion thereof which supports the connecting lead portion.

17. The semiconductor device according to claim 15, wherein each of the first and the second semiconductor chip includes a MOSFET and the first semiconductor chip further includes a Schottky diode connected in parallel with the MOSFET.

18. The semiconductor device according to claim 15, wherein the tie bar is made smaller in thickness than other portions of the inner leads.

19. The semiconductor device according to claim 15, wherein the tie bar is provided midway on and

between the external leads to which the two inner leads are connected.

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20. The semiconductor device according to claim 15, wherein the die pad has a notch in a portion that faces the tie bar.

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